**Course :** B.Tech **Year / Semester:** 2/1

**Subject Name : Computer Organization and Architecture**

**Branch Name(s):** CSE, CSE(AIML), CSE(DS), AIDS

**Subject Code(s) :** 23CS303PC, 23CA301PC, 23CD303PC, 23AI305PC

**DESCRIPTIVE QUESTION BANK**

**UNIT – I**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QNO** | **Description of Question** | **Marks** | **CO** | **PO** | **BTL** |
| 1 | Design and implement arithmetic Micro-Operations in CPU Architecture | 5 | 1 | 2 | 6 |
| 2 | Design a common bus for four registers of four bits each using multiplexers | 5 | 1 | 3 | 6 |
| 3 | A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.  i)How many bits are there in the operation code, the register code part, and the address part?  ii) Draw the instruction word format and indicate the number of bits in each part.  iii)How many bits are there in the data and address inputs of the memory? | 5 | 1 | 1 | 5 |
| 4 | Design and implement the basic computer instruction cycle. | 5 | 1 | 2 | 6 |
| 5 | Design the basic computer instructions. | 5 | 1 | 3 | 6 |

**UNIT-2**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QNO** | **Description of Question** | **Marks** | **CO** | **PO** | **BTL** |
| 1 | A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, all connected to a common bus system.  i). Formulate a control word for a micro operation.  ii). Specify the number of bits in each field of the control word and give a general encoding scheme.  iii). Show the bits of the control word that specify the micro operation R4🡨R5 + R6. | 5 | 2 | 1 | 5 |
| 2 | Design symbolic microprograms for FETCH, ADD, BRANCH, STORE | 5 | 2 | 1 | 6 |
| 3 | Design the programs to evaluate the following arithmetic statement using zero, one, two and three address instructions. Use the conventional symbols and instructions. X = (A\*B) / (C\*D). | 5 | 2 | 2 | 6 |
| 4 | An instruction is stored at location 300 with its  address field at location 301 . The address field  has the value 400. A processor register R1  contains the number 200. Evaluate the effective  address if the addressing mode of instruction is  (i) direct; (ii) immediate; (iii) relative; (iv) register  indirect; (v) index with R1 as the index register. | 5 | 2 | 1 | 5 |
| 5 | Design the microprogram sequencer for a control memory. | 5 | 2 | 2 | 6 |

**UNIT-3**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QNO** | **Description of Question** | **Marks** | **CO** | **PO** | **BTL** |
| 1 | Design the algorithm for addition and subtraction with signed magnitude numbers. | 5 | 3 | 3 | 4 |
| 2 | Design the Booth’s Multiplication algorithm and demonstrate with numerical example. | 5 | 3 | 2 | 6 |
| 3 | Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders. | 5 | 3 | 1 | 6 |
| 4 | Design the algorithm for addition and subtraction with floating point numbers. | 5 | 3 | 2 | 5 |
| 5 | Design the algorithm for addition and subtraction with signed 2’s complement representation and demonstrate by performing the arithmetic operations (+42) + ( -13) and (- 42) - ( -13) in binary using signed 2’s complement representation for negative numbers. | 5 | 3 | 2 | 3 |

**UNIT-4**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QNO** | **Description of Question** | **Marks** | **CO** | **PO** | **BTL** |
| 1 | A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used.  The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.   1. How many RAM and ROM chips are needed? 2. Draw a memory-address map for the system. 3. Give the address range in hexadecimal for RAM, ROM, and interface | 5 | 4 | 3 | 5 |
| 2 | Design a parallel priority interrupt hardware for a system with eight interrupt sources | 5 | 4 | 2 | 6 |
| 3 | Design strobe control and hand shaking methods | 5 | 4 | 1 | 4 |
| 4 | Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64Kwords which are divided into 8192 blocks of 8 words each.   1. Find the number of bits in Tag, Block, Word field of the main memory address for direct mapping scheme. 2. Find the number of bits in Tag, Word field of the main memory address for Associate mapping scheme. 3. Find the number of bits in Tag, Set , Word field of the main memory address for set associate mapping scheme. | 5 | 4 | 2 | 4 |
| 5 | Design the match logic for one word of Associative Memory and draw the logic diagram. | 5 | 4 | 3 | 6 |

**UNIT-5**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QNO** | **Description of Question** | **Marks** | **CO** | **PO** | **BTL** |
| 1 | A non-pipeline system takes 50 ns to process a task. The same task can be in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved? | 5 | 5 | 2 | 4 |
| 2 | In a certain scientific computation, it is necessary to perform the arithmetic operation (Ai + Bi) (Ci + Di) with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. | 5 | 5 | 3 | 5 |
| 3 | Design and implement a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. | 5 | 5 | 3 | 6 |
| 4 | Design the pipeline for addition and subtraction with floating point numbers. | 5 | 5 | 2 | 6 |
| 5 | Design the three stage RISC pipeline. Give an example of a program that will cause data conflict in the three-segment pipeline and how it is resolved. | 5 | 5 | 2 | 6 |

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**OBJECTIVE QUESTION BANK**

**UNIT – I**

**Multiple Choice Questions:**

1.Computer Organization is concerned with [ ]

* 1. The way hardware components operate and connected together to form Computer system.
  2. The determination of what hardware should be used and how the parts be connected.
  3. The structure and behavior of the computer as seen by the user.
  4. Design of electronic components of computer.

2. The part of the hardware of computer that controls the transfer of information between

computer and the outside word is [ ]

a)CPU b)Memory c)IOP d)Microprocessor

3. In direct addressing mode address part of instruction specifies [ ]

a)Address of next instruction b)Address of register

c)Address of operand in memory d)Operand itself

4. In indirect addressing mode address part of instruction specifies [ ]

a)Address of next instruction b)Address of current instruction

c)Address of operand d)Address of memory location containing address of operand

5. The memory reference instruction that denotes operation PC 🡨AR is [ ]

1. AND b) BSA c) BUN d)STA

6. The transfer of information from a memory word to the outside environment is called a \_\_\_\_\_\_\_\_ operation. [ ]

a) Read b) write c) both d) none

7. To design a common bus system for 4 register of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder? [ ]

a) 2 to 4 Decoder b) 3 to 8 Decoder c) 4 to 16 Decoder d)5 to 32 decoder

8. If the address field of an instruction specifies the effective address, then the instruction is

[ ]

a) Immediate Instruction b) Direct Instruction c) Indirect Instruction d) None

9 There are \_\_\_\_\_\_\_\_\_\_\_ different logical operations that can be performed with 2 binary variables [ ]

1. 2 b) 4 c) 8 d) 16.

10. In the Binary Adder/subtractor if M=0 the circuit is \_\_\_\_\_\_\_\_\_\_ [ ]

a) adder b) subtractor c) both adder & subtractor d) exclusive Binary Operation.

11. The \_\_\_\_\_\_\_\_\_ operation is similar to the selective clear operation except that the bits of A are cleared only where there are corresponding 0's in B. [ ]

a) Selective – set b) Selective – complement c) Mask d) Insert .

**Fill in the blanks:**

12. The type of shift used to shift the contents of a register which contains a signed binary number is called \_\_\_\_\_\_\_\_\_\_\_

13. If the memory size is 4096\*16, then \_\_\_ address lines are required to address any memory location

14. The \_\_\_\_\_\_\_\_\_\_\_\_\_\_ operation sets to 1 bit in register A where there are corresponding 1’s in register B.

15. Description of SPA instruction \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

16. An \_\_\_\_\_\_\_\_\_\_\_\_\_ is s a group of bits that instruct the computer to perform a specific operation.

17. A \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is a fast electronic calculating machine that accepts digitized input information, processes it according to a list of internally stored instructions and the resulting output information.

18. The \_\_\_\_\_\_\_\_\_\_\_\_ holds the address of the next instruction to be read from memory after the current instruction is executed.

19. An elementary operation performed on the information stored in one or more registers is referred as \_\_\_\_\_\_\_\_\_\_\_

20. A common bus for eight registers of 16 bits each requires \_\_\_\_\_\_\_ number of multiplexers.

21. An arithmetic shift right \_\_\_\_\_\_\_\_ the signed binary number by 2. An arithmetic shift left \_\_\_\_\_\_\_ a signed binary number by 2.

22.\_\_\_\_\_\_\_\_\_\_ holds the address of the memory location to be accessed

23. \_\_\_\_\_\_\_\_\_\_\_\_\_\_ holds the instruction code that is currently being executed.

**UNIT-1 Key:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qno** | **Answer** | **Qno** | **Answer** |
| **1** | **A** | **13** | **12** |
| **2** | **C** | **14** | **Selective set** |
| **3** | **C** | **15** | **Skip the next instruction if AC is positive** |
| **4** | **D** | **16** | **Instruction code** |
| **5** | **C** | **17** | **Digital computer** |
| **6** | **A** | **18** | **Program counter** |
| **7** | **A** | **19** | **Microoperation** |
| **8** | **B** | **20** | **16** |
| **9** | **D** | **21** | **Divides, Multiplies** |
| **10** | **A** | **22** | **Address register** |
| **11** | **C** | **23** | **Instruction Register** |
| **12** | **Arithmetic shift** |  |  |

**UNIT – 2**

1. The control logic is implemented with gates, flip-flops, decoders, and other digital circuits. [ ]

a) Hardwired control b) Microprogrammed c)Control logic d)None

2. If the control signals are generated using hardware with conventional logic design techniques then the control unit is said to be [ ]

a)Micro programmed b)Hardwired

c)Nano programmed d)Programmed

3. The register used to store return address of sub routine is [ ]

a)Control address Register (CAR) b)Sub routine register (SBR)

c)Instruction register (IR) d)Program counter (PC)

4. Micro instructions are stored in [ ]

a)Main memory b)Secondary memory c)Control memory d)Virtual memory

5. The memory reference instruction that denotes operation AC 🡨M[AR] is [ ]

a)AND b)BSA c)BUN d)LDA

6. RPN is also called as [ ]

a) Infix Notation b) Polish Notation c) Prefix Notation d) Postfix Notation

7 \_\_\_\_\_\_\_\_\_ refer to the transfer of program control from a currently running program to another service program as result of external or internal generated request. [ ]

a)Program Interrupt b) Internal Interrupt c) External Interrupt d) Software Interrupt

8. Postfix notation of (A+B)\*C is [ ]

a. AB+\*C b. AB\*+C c . ABC+\* d. AB+C\*

9 Stack follows the \_\_\_\_\_\_\_\_\_\_ operation [ ]

a) L I F O b) F I F O c) S J F d) none

10 Which of the following is shift instruction [ ]

a) RORC b) CALL C) SKP d) SETC

**Fill in the blanks:**

11. The next address generator is also called as \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

12 In the Micro instruction code Format the condition field consists of two bits which are encoded to specify\_\_\_\_\_\_\_ status bit conditions

13 A \_\_\_\_\_\_\_\_\_\_\_\_\_ requires changes in the wiring among the various components if the design has to be modified (or) changed.

14. The transformation from the instruction code bits to an address in control memory where the routine located is referred as \_\_\_\_\_\_\_\_\_\_

15. In Micro programmed organization, the control information is stored in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

16. A control unit whose binary control variables are stored in memory is called \_\_\_\_\_\_\_\_\_\_\_\_\_ control unit

17 The register that holds the address for the stack is called \_\_\_\_\_\_\_\_\_\_

18 Internal interrupts are also called as \_\_\_\_\_\_\_\_\_\_\_

19 The implied operand of an operation in a single accumulator organization is \_\_\_\_\_\_\_\_\_\_\_\_\_

20.In a memory stack, after the pop operation, the stack pointer will be \_\_\_\_\_\_\_\_\_\_\_\_

**UNIT-2 Key:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qno** | **Answer** | **Qno** | **Answer** |
| **1** | **A** | **11** | **Microprogram Sequencer** |
| **2** | **B** | **12** | **4** |
| **3** | **B** | **13** | **Hardwired control unit** |
| **4** | **C** | **14** | **Mapping process** |
| **5** | **D** | **15** | **Control memory** |
| **6** | **D** | **16** | **microprogrammed** |
| **7** | **A** | **17** | **Stack pointer** |
| **8** | **D** | **18** | **traps** |
| **9** | **A** | **19** | **accumulator** |
| **10** | **A** | **20** | **incremented** |

**UNIT – 3**

1.Binary coded decimal number for 99 is \_\_\_\_\_\_\_\_ [ ]

a) 1100011 b) 00110101 c) 10011001 d) 00100000.

2. In the Hardware for Signed –Magnitute addition and subtraction two magnitudes are subtracted if the sign are different for an \_\_\_\_\_\_\_\_ Operation (or) identical for an \_\_\_\_\_\_\_\_ operation. [ ]

a) add , subtract b) add , Multiply c) subtract , add d) Multiply , add.

3. Convert the following binary number into decimal 101110 [ ]

a) 55 b) 45 c)46 d)56

4. Obtain the 10’s complement of the following 6-bit decimal number 100000 [ ]

a. 999999 b. 899999 c. 900000 d. 100000

5. What is the description about following decimal arithmetic microoperation? QL 🡨 QL+1 [ ]

a.Increment QL register b. Increment BCD number in QL

c. Increment decimal number in QL  d. All the above

6. Convert the hexadecimal number F3A7C2 to binary [ ]

a.111101101101100010101001 b. 111111000101101101011110

c. 111100111010011111000010 d. 111110011001100000010010

7. Perform the subtraction with the following unsigned decimal number by [ ]

taking the 10’s complement of the subtrahend 1200-250.

a. 450 b. 950 c. 749 d. 449

8. N-bit sign magnitude numbers can represent quantities from [ ]

a) –(2(n-1)-1) to +(2(n-1)) b) –(2(n-1)-1) to +(2(n-1)-1) c) –(2n-1) to +(2n-1) d) –(2n-1) to +2n

9.What is the 8-bit 2’s complement of -12 [ ]

a. 1111 0100 b. 1000 1100 c. 0000 0100 d. 0000 0011

10. If (123)5=(x3)y, then the number of possible values of x is [ ]

a. 4 b. 1 c. 3 d. 2

**Fill in the blanks:**

11. A floating- point number is said to be \_\_\_\_\_\_\_\_\_\_\_\_\_if the most- significant digit of the mantissa is nonzero.

12The Divisor is shifted once to the right and subtracted from the dividend. That difference is called a \_\_\_\_\_\_\_\_\_\_\_\_\_\_.

13The r’s complement of an n-digit number N in base r is defined as \_\_\_\_\_\_\_\_\_\_\_\_\_

14. The decimal equivalent of the binary number 101.101 is \_\_\_\_\_\_\_\_\_\_\_\_\_

15. The 9’s complement of BCD (1001) is \_\_\_\_\_\_\_\_\_\_\_\_\_

16. In BCD addition, when the binary sum is greater than 1001, then addition of \_\_\_\_\_\_\_ converts the binary sum to correct BCD representation

17 An n-bit 2’s complement number can represent values \_\_\_\_\_\_\_\_\_\_\_\_\_

18. In a Array multiplier circuit with ‘j’ multiplier bits and ‘k’ multiplicand bits, the number of

AND gates required are \_\_\_\_\_\_\_\_\_\_\_

19. A divide overflow condition occurs, if the high order half bits of the dividend is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

20. \_\_\_\_\_\_\_\_\_\_\_ algorithm specifies a procedure for multiplying two binary integers in Signed 2’s complement.

**UNIT-3 Key:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qno** | **Answer** | **Qno** | **Answer** |
| **1** | **C** | **11** | **normalized** |
| **2** | **A** | **12** | **Partial remainder** |
| **3** | **C** | **13** | **rn-N** |
| **4** | **C** | **14** | **5.625** |
| **5** | **B** | **15** | **0000** |
| **6** | **C** | **16** | **0110** |
| **7** | **B** | **17** | **–(2 (n-1) ) to +(2 (n-1) -1)** |
| **8** | **B** | **18** | **J \* K** |
| **9** | **A** | **19** | **Greater than or equal to the divisor** |
| **10** | **D** | **20** | **Booth’s Multiplication** |

**UNIT-4**

1. Machines whose instructions generate 32-bit address can utilize a memory that contains up to \_\_\_\_\_\_\_ memory locations [ ]

A. 28  B. 216  C. 232  D. 248

2. The CPU has distinct i/p and o/p instructions and each of these instructions is associated with the address of an interface register. [ ]

A. Memory Mapped I/O B. I/O Port C. Isolated I/O D. I/O Command

3. Backup storage is called as [ ]

A. Cache Memory B. Main Memory C. Auxiliary Memory D. Virtual Memory

4. Baud rate is data transfer in [ ]

A.bits per second B. bytes per second C. words per second D. all the above

5. During a \_\_\_\_\_\_\_\_\_ operation, the sense/read circuits, the information stored in the cells selected by a word line and transmit this information to the o/p data lines [ ]

A. Write B. Read C. Read/Write D. Write & Read/Write

6. The interface transfer s data into and out of the memory unit through the memory bus. [ ]

1. Programmed-I/O B. Interrupted-Initiated I/O C. Direct Memory Access D. all the above

7In the \_\_\_\_\_\_\_\_\_\_\_\_ only the cache is updated and the location is marked so that it can be copied later into main memory. [ ]

1. Write through policy B. Cache Coherence C. Write- back policy D. Cache Incoherence

8. Many instructions in localized areas of the program are executed repeatedly during some time period, and the remainder of the program is accessed relatively infrequently . [ ]

A. Locality reference B. spatial C. temporal D. cache

9. Which of the following is volatile? [ ]

A) Bubble memory B) RAM C) ROM D) Magneticdisk

10. In a non-vectored interrupt [ ]

A) The branch address is assigned to a fixed location in memory

B)The interrupting source supplies the branch information to the processor through an interrupt vector

C)The branch address is obtained from a register in the process

D)Both The interrupting source supplies the branch information to the processor through an interrupt vector & The branch address is obtained from a register in the process

**Fill in the blanks:**

11 In an **\_\_\_\_\_\_\_\_\_\_\_\_\_** different sets of addresses are assigned to different memory locations.

12. The bus grant signal is replaced by a set of lines called poll lines which are connected to all units is called as **\_\_\_\_\_\_\_\_\_\_\_\_**

13 Expand UART: **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

14 The number of hits stated as a fraction of all attempted accesses is called **\_\_\_\_\_\_\_\_\_\_\_\_**

15. In the **\_\_\_\_\_\_\_\_\_\_\_\_\_** policy, both cache and main memory are updated with every write operation.

16Input-Output interface provides a method for transferring information between **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

17The DMA controller to transfer one data word at a time, after which it must return control of the buses to the cpu, this technique is called as **\_\_\_\_\_\_\_\_\_\_\_\_**

18. Associative memory is called **\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

19 A serial transmission technique which employs special bits to mark the ends of character is called **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

20 If the branch address of the interrupt routine is supplied by the source it is called **\_\_\_\_\_\_\_\_\_\_\_\_** interrupt.

**UNIT-4 Key:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qno** | **Answer** | **Qno** | **Answer** |
| **1** | **C** | **11** | **Interleaved memory** |
| **2** | **C** | **12** | **polling** |
| **3** | **C** | **13** | **Universal Asynchronous Receiver Transmitter** |
| **4** | **A** | **14** | **Hit Ratio** |
| **5** | **B** | **15** | **Write through** |
| **6** | **C** | **16** | **Internal storage and external i/o devices** |
| **7** | **C** | **17** | **Cycle stealing** |
| **8** | **A** | **18** | **Content addressable memory** |
| **9** | **B** | **19** | **Asynchronous transfer** |
| **10** | **A** | **20** | **vectored** |

**UNIT-5**

1. The speed up of a pipeline processing over an equivalent non-pipeline processing is defined by the ratio S =\_\_\_\_\_\_\_\_\_ [ ]

A. ntn /(k+n-1)tp B. ntp/(k+n-1)tn C.ntn /(k+n+1)tp D.ntp/(k-n-1)tn

2 Which of the following is a type of array processors? [ ]

a) Super array processor b) MISD array processor   
c) SIMD array processor d) All of above

3. Application of Vector Processing is [ ]

A. Library System B. Medical Diagnosis C. Seismic Wave Analysis D. Space Research

4 An \_\_\_\_\_\_\_\_\_\_ is an auxiliary processor attached to a general purpose computer . [ ]

1. SIMD array Processor B. Attached array Processor C. Vector Processor D. All the above

5. An \_\_\_\_\_\_\_\_\_\_\_\_\_\_is a processor that as single instruction multiple data organization [ ]

A. SIMD array Processor B. Attached array Processor C. Vector Processor D. All the Above

6. To compute n-tasks using a k-segments pipeline requires \_\_\_\_\_\_ clock cycles [ ]

A. k-(n+1) B. k-(n-1) C. k+ (n-1) D. k+ (n+1)

7. The \_\_\_\_\_\_\_\_\_ algorithm allocates a fixed –length time slice of bus time that is offered sequentially to each processor. [ ]

1. FIFO B. LRU C. Time slice D. Polling

8. \_\_\_\_\_\_\_\_\_ arise from branch and other instructions that change the value of pc [ ]

A. Data Dependency B. Resource conflict C. Branch difficulties D. NONE

9\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ caused by access to memory by two segments at the same time [ ]

1. Data dependency B. Resource Conflict C. Branch difficulties D. Delay load

10. Which of the following is not valid segment of three-stage instruction pipeline in RISC?

a) I b) A c)E d)F [ ]

**Fill in the blanks:**

11 **\_\_\_\_\_\_\_\_\_\_\_\_** is a technique of decomposing a sequential process into sub operations, with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

12 An **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** operates on a stream of instructions by overlapping the fetch, decode and execute phases of the instruction cycle.

13A **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** is a program sequence that, once begun, must complete execution before another processor access the same shared resource.

14 Expand SIMD **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

15. Multi processors and Multi computer system come into **\_\_\_\_\_\_\_\_\_\_\_\_** category

16 \_\_\_\_\_\_\_\_\_\_\_\_\_is the solution of branch difficulties that is mostly used in RISC computers.

17 A measure used to evaluate [computers](https://gtu-mcq.com/BE/Computer-Engineering/Semester-4/3140707/5260/MCQs?q=62pxAP7c7zo=) in their ability to perform a given number of floating-point operations per second is referred to as \_\_\_\_\_\_.

18 Attached array processor is generally direct connected with \_\_\_\_\_\_\_\_\_ & \_\_\_\_\_\_\_\_\_\_\_.

19. The bus controller that monitors the cache coherence problem is referred as **\_\_\_\_\_\_\_\_\_\_\_\_\_**

20 Each processor element in a **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** system has its own private local memory

**UNIT-5 Key:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qno** | **Answer** | **Qno** | **Answer** |
| **1** | **A** | **11** | **Pipelining** |
| **2** | **C** | **12** | **Instruction pipeline** |
| **3** | **B** | **13** | **Critical section** |
| **4** | **B** | **14** | **Single Instruction Stream Multiple Data Stream** |
| **5** | **D** | **15** | **MIMD** |
| **6** | **B** | **16** | **Delayed branch** |
| **7** | **C** | **17** | **FLOPS** |
| **8** | **C** | **18** | **I/O interface, Local memory** |
| **9** | **B** | **19** | **Snoopy cache controller** |
| **10** | **D** | **20** | **Loosely copuled** |